



K-Band Power Embedded Transmission Line (ETL) MMIC Amplifiers for Satellite Communication Applications

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Prepared for the
1999 Radio Frequency Integrated Circuit (RFIC) Symposium
sponsored by the Institute of Electrical and Electronics Engineers
Anaheim, California, June 13–15, 1999

Prepared under Cooperative Agreement NCC3–497

National Aeronautics and
Space Administration

Lewis Research Center

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K-BAND POWER EMBEDDED TRANSMISSION LINE (ETL) MMIC AMPLIFIERS FOR SATELLITE COMMUNICATION APPLICATIONS

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Abstract

The design, fabrication, and performance of K-band high-efficiency, linear power pHEMT amplifiers implemented in Embedded Transmission Line (ETL) MMIC configuration with unthinned GaAs substrate and top-side grounding are reported. A three-stage amplifier achieved a power-added efficiency of 40.5% with 264 mW output at 20.2 GHz. The linear gain is 28.5 dB with 1-dB gain compression output power of 200 mW and 31% power-added efficiency. The carrier-to-third-order intermodulation ratio is ~ 20 dBc at the 1-dB compression point. A RF functional yield of more than 90% has been achieved.

Summary

Emerging mobile satellite communication systems require MMIC components that are efficient, small-size, and suitable for low-cost antenna array implementations. Our Embedded Transmission Line (ETL) MMIC concept first reported in [1] utilizes matching circuits with transmission lines and lumped passive components (resistors, series/shunt capacitors, and spiral inductors) embedded in a low-K dielectric (polyimide) medium coated over the active devices. The quasi-hermetic nature of the ETL MMIC simplifies the packaging requirement. Highly uniform performance from a K-band low-noise amplifier design and state-of-the-art noise performance from a Ka-band MMIC design were reported [2]. In this paper, we further report the development of power ETL MMIC amplifiers suitable for spaceborne phased array antenna implementation using flip-chip mounting technique in multilayer circuits [3]. AlGaAs/InGaAs on GaAs pseudomorphic high electron mobility transistor (pHEMT) with $0.25\text{ }\mu\text{m}$ long T-gate was used. The ETL MMIC design is based on $25\text{ }\mu\text{m}$ thick polyimide and 25-mil thick GaAs substrate. No backside processing such as substrate thinning, plating, and through-substrate vias is required. This greatly simplifies the processing steps and reduces the production cost. **Figure 1** shows the dual-channel K-band three-stage ETL MMIC power amplifiers with a chip size of 100×180 mils. Two identical amplifiers are laid out side by side on the same chip to simplify array packaging. Several designs with different device sizes were used to meet the different power element requirement of the array. The circuit designs are such that the same RF I/O's and bias pad locations are used to simplify the module routing requirements. The top picture shows the top-side ground with RF I/O's and bias pads. The bottom picture shows the under-lying circuitry with the top $25\text{-}\mu\text{m}$ thick polyimide layer removed. With the exception of RF input/output pads and gate/drain pads, a solid ground plane is available for ease of connecting to other components without bondwires.

One three-stage amplifier design has cascaded $100\text{ }\mu\text{m}/300\text{ }\mu\text{m}/600\text{ }\mu\text{m}$ gate width pHEMTs. **Figure 2** shows a SEM photograph of the output $600\text{ }\mu\text{m}$ device prior to the polyimide coating. The device size ratio was chosen, based on trade-off among gain, efficiency, power, and intermodulation distortion requirements. Optimum source and load impedance from large-signal load-pull and third-order intermodulation load-pull were used in the amplifier designs. The on-chip bias network allows the use of a single gate voltage and a single drain voltage for power supply requirement simplification in modules. On-wafer small-signal and large-signal characterizations, including two-tone distortion were performed on both discrete devices and MMIC amplifiers. Since the devices and MMICs were not flipped (i.e., topside ground with the heat flows through the thick GaAs substrate), even better performance than that reported here with the on-wafer characterization should be achievable, once the wafer is diced and MMIC flip-chip mounted.

Figure 3 shows the small-signal gain-frequency response of four amplifiers with each taken from four different 3-inch wafers biased at the same gate and drain voltages. It is seen that the response is very uniform over the design bandwidth of 19 GHz to 22 GHz. With a drain voltage of 3 V, the gain is 27 to 30 dB. **Figure 4** shows the power performance of the amplifier as a function of input drive level. The linear gain is nearly 30 dB (at 19 GHz) with a power-added efficiency of 40.5% with 264 mW output at 20.2 GHz. The 1-dB gain compression output power is 200 mW with 31% PAE. It is to be noted that these excellent results can be achieved with a drain bias of only 5 V. With flip-chip mounting and a higher drain voltage, even higher output power is expected. **Figure 5** shows the two-tone test with 0.5 MHz separation for the two signals at 19 GHz at a drain bias of 5 V and two different gate biases (i.e., -0.4 V and -0.5V). At 1-dB gain compression, the C/I3 ratio is ~ 20 dBc. At 5-dB back-off from saturation, the C/I3 ratio is ~ 28 dBc. Other amplifiers with output device of 1200 μm gatewidth had up to 500 mW output at 19 GHz with scaled C/I3 performance. RF functional yield as high as 90% was achieved on these amplifiers.

****Work supported in part by NASA Lewis Research Center, Cleveland, Ohio under Cooperative Agreement No. NCC3-497.**

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- [1] H. Q. Tserng, Paul Saunier, Andrew Ketterson, Larry Witkowski, and Ted Jones, "Embedded Transmission Line (ETL) MMIC for Low-Cost, High-Density Wireless Communication Applications", IEEE Transactions on Microwave Theory and Techniques, vol.45, No. 12, December 1997, pp.2540-2548
- [2] H. Q. Tserng, L. Witkowski, A. Ketterson, P. Saunier, and T. Jones, "K/Ka-Band Low-Noise Embedded Transmission Line (ETL) MMIC Amplifiers," 1998 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Digest of Papers, pp. 183-186
- [3] T. Budka, A. Ketterson, H.-Q. Tserng, L. Stiborek, L. Heinrich, R. Smith, B. Ables, C. Kyhl, K. Worthen, G. Brehm, and J. Reddick, "Embedded Transmission Line MMIC 1-W Flip Chip Assembly Using a Z-axis Interconnect," IEEE Microwave and Guided Wave Letters, June 1998, pp. 238-240.

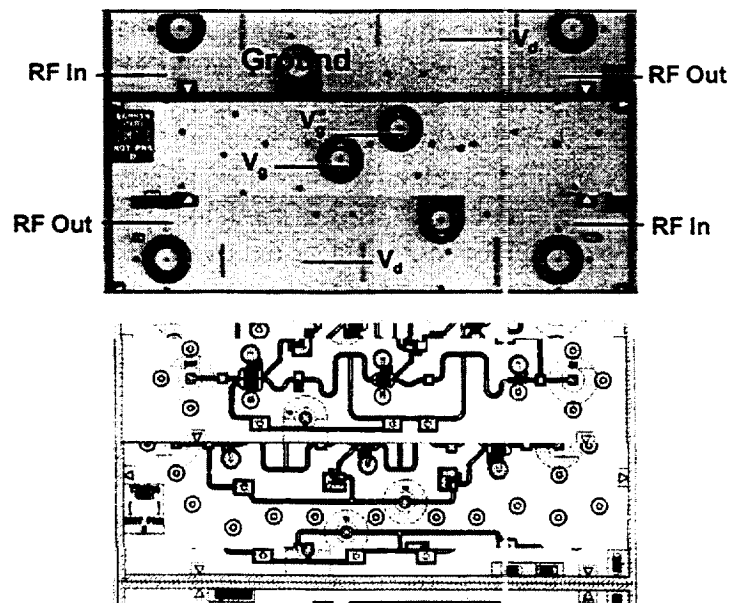


Figure 1: K-Band Dual-Channel ETL pHEMT MMIC Power Amplifiers

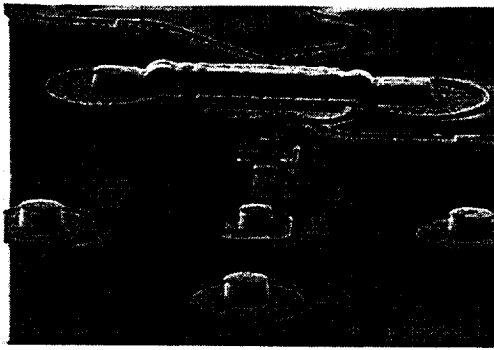


Figure 2: SEM Photo Taken on the Output 600 μm Device Prior to Polyimide Coating

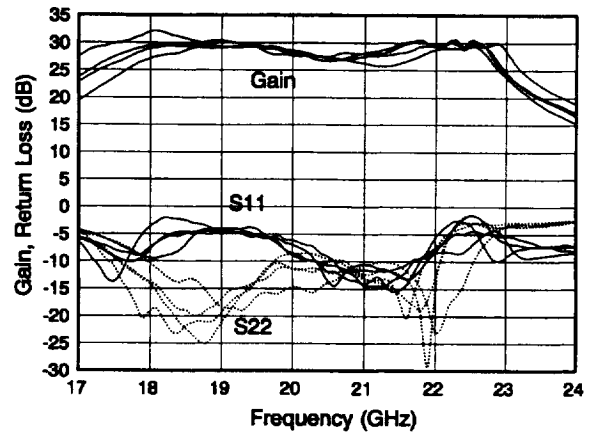


Figure 3: Small-Signal Gain-Frequency Response of MMICs from Four Wafers ($V_g = -0.5\text{ V}$, $V_d = 3\text{ V}$, $I_d \sim 100\text{ mA}$)

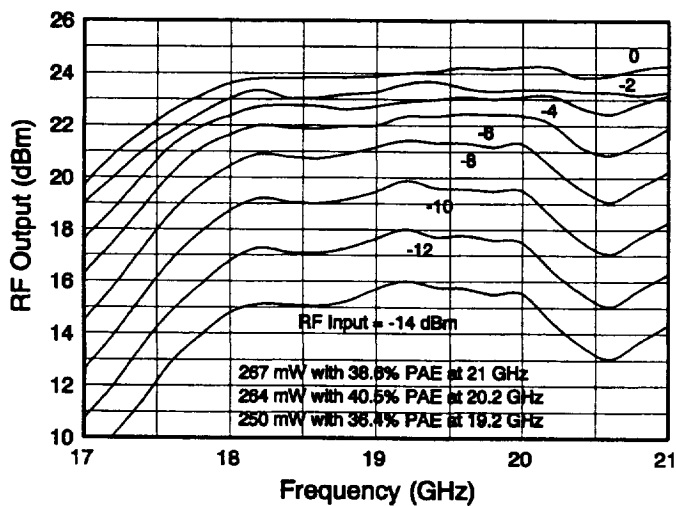


Figure 4: Performance of a Three-Stage K-Band ETL MMIC Amplifier ($V_g = -0.5\text{ V}$, $V_d = 5\text{ V}$, $I_d \sim 125\text{ mA}$)

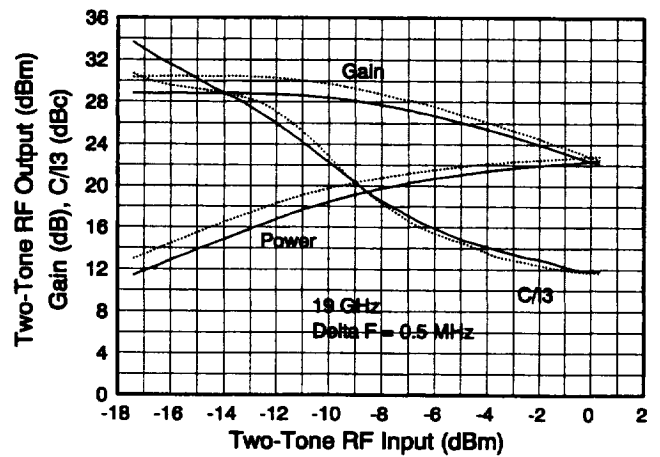


Figure 5: Gain Compression and Two-Tone Distortion Characteristics of a K-Band ETL MMIC Amplifier ($V_d = 5\text{ V}$, solid line: $V_g = -0.5\text{ V}$, $I_q = 123\text{ mA}$, dotted line: $V_g = -0.4\text{ V}$, $I_q = 160\text{ mA}$)

REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188	
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.				
1. AGENCY USE ONLY (Leave blank)		2. REPORT DATE November 1998		3. REPORT TYPE AND DATES COVERED Final Contractor Report
4. TITLE AND SUBTITLE K-Band Power Embedded Transmission Line (ETL) MMIC Amplifiers for Satellite Communication Applications			5. FUNDING NUMBERS WU-632-50-5B-00 NCC3-497	
6. AUTHOR(S) Hua-Quen Tserng, Andrew Ketterson, Paul Saunier, Larry McCarty, and Steve Davis				
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Raytheon System Company P.O.Box 869305 Plano, Texas 75086			8. PERFORMING ORGANIZATION REPORT NUMBER E-11420	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) National Aeronautics and Space Administration Lewis Research Center Cleveland, Ohio 44135-3191			10. SPONSORING/MONITORING AGENCY REPORT NUMBER NASA CR-1998-208681	
11. SUPPLEMENTARY NOTES Hua-Quen Tserng, Andrew Ketterson, and Paul Saunier, TriQuint Semiconductor Company, Dallas, Texas; Larry McCarty, and Steve Davis, Raytheon System Company. Project Manager, Godfrey Anzic, Communications Technology Division, NASA Lewis Research Center, organization code 5640, (216) 433-3570.				
12a. DISTRIBUTION/AVAILABILITY STATEMENT Unclassified - Unlimited Subject Categories: 17 and 33 Distribution: Nonstandard This publication is available from the NASA Center for Aerospace Information, (301) 621-0390.			12b. DISTRIBUTION CODE	
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14. SUBJECT TERMS MMIC; Amplifiers; K-band; pHEMT; ETL; Satellite communications			15. NUMBER OF PAGES 9	
			16. PRICE CODE A02	
17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT	